

WHAT IS CLAIMED IS:

1. A data transferring apparatus for transferring liquid ejection data, comprising:

a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development; and

an invalid data mask processing means for nullifying data from head data, as many bytes as a remainder resulting from dividing a value of a data starting address of compressed liquid ejection data by the number of data bytes which said system bus can transfer per one data transfer, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

2. A data transferring apparatus for transferring liquid ejection data, comprising:

a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development; and

an invalid data mask processing means for nullifying head data of one byte in case data starting address of compressed data stored in said main memory is an odd address, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

3. A data transferring apparatus for transferring liquid ejection data as claimed in claim 1 or 2, further comprising:

two independent buses which are said system bus and a local

bus;

said main memory coupled to said system bus, capable of transferring data;

a local memory coupled to said local bus, capable of transferring data; and

a decode unit coupled to said system bus and local bus in order to transfer data therebetween, comprising:

a decode circuit;

a line buffer for storing liquid ejection data developed by said decode circuit per word unit; and

a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit, DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially.

4. A data transferring apparatus for transferring liquid ejection data as claimed in claim 3, wherein an ASIC comprises registers of said main memory, said decode unit and said liquid ejecting head as a circuit block respectively, and registers of said decode unit and said liquid ejecting head are coupled through an dedicated bus in said ASIC.

5. A data transferring apparatus for transferring liquid ejection data as claimed in claim 4, wherein said line buffer comprises two faces of buffer areas capable of storing developed data of predetermined words, liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas while liquid ejection data developed by said decode

circuit is sequentially stored in a second face of said buffer areas when developed data of predetermined words has been accumulated, and developed data is DMA-transferred to said local memory per predetermined words when developed data of predetermined words has been accumulated.

6. A data transferring apparatus for transferring liquid ejection data as claimed in claim 5, wherein data transfers with respect to said local bus from said decode circuit to said local memory and from said local memory to a register of said liquid ejecting head are performed in a burst transfer.

7. A data transferring apparatus for transferring liquid ejection data as claimed in claim 6, wherein said compressed liquid ejection data is run length compressed data, and said decode circuit can perform hardware development on run length compressed data.

8. A data transferring apparatus for transferring liquid ejection data as claimed in claim 7, wherein said decode unit comprises a non-development processing means for storing uncompressed liquid ejection data DMA-transferred from said main memory in said line buffer without hardware development by said decode circuit.

9. A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data comprising:

a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development; and

an invalid data mask processing means for nullifying data

from head data, as many bytes as a remainder resulting from dividing a value of a data starting address of compressed liquid ejection data by the number of data bytes which said system bus can transfer per one data transfer, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

10. A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data comprising:

a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development; and

an invalid data mask processing means for nullifying head data of one byte in case data starting address of compressed data stored in said main memory is an odd address, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

11. A data transferring apparatus for transferring liquid ejection data, comprising:

a decode unit comprising a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;

a line buffer for storing liquid ejection data developed by said decode circuit per word unit and a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit; and

DMA-transferring liquid ejection data developed in said line

buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially,

wherein said decode unit comprises a data rearranging means for storing data in an array direction of a bitmap for a liquid ejecting head corresponding to a nozzle array of a liquid ejecting head in said local memory, when data developed in said line buffer is DMA-transferred to a bitmap area of said local memory per word unit.

12. A data transferring apparatus for transferring liquid ejection data as claimed in claim 11, wherein said decode unit comprises a data dividing means for storing data in bitmap areas which are different per predetermined words, when data developed in said line buffer is DMA-transferred to a bitmap area of said local memory per word unit.

13. A data transferring apparatus for transferring liquid ejection data as claimed in claim 12, wherein said data dividing means sets the number of bitmap areas to be divided in accordance with a ratio of the resolution of liquid ejection data and the resolution of said liquid ejecting head.

14. A data transferring apparatus for transferring liquid ejection data as claimed in claim 13, wherein said data transferring apparatus comprises an invalid data mask processing means for nullifying data from head data, as many bytes as a remainder resulting from dividing a value of a data starting address of compressed liquid ejection data by the number of data bytes which said system bus can transfer per one data transfer, with respect to word data including head data of compressed data DMA-transferred

from said main memory to said decode circuit.

15. A data transferring apparatus for transferring liquid ejection data as claimed in claim 13, wherein said data transferring apparatus comprises an invalid data mask processing means for nullifying head data of one byte in case data starting address of compressed data stored in said main memory is an odd address, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

16. A data transferring apparatus for transferring liquid ejection data as claimed in claim 15, wherein said decode unit comprises a data storage starting position shifting means for storing liquid ejection data developed by said decode circuit from a first byte of said line buffer in a state where a 0-th byte of said line buffer is vacant.

17. A data transferring apparatus for transferring liquid ejection data as claimed in claim 16, wherein said decode unit comprises a data storage ending position shifting means for transferring developed liquid ejection data stored in said line buffer to liquid ejecting head each time developed data of said predetermined words from which one byte has been subtracted is stored in said line buffer.

18. A data transferring apparatus for transferring liquid ejection data as claimed in claim 17, wherein said data transferring apparatus comprises two independent buses which are said system bus and a local bus, said main memory coupled to said system bus, capable of transferring data and said local memory coupled to said local bus, capable of transferring data, and said decode unit is

coupled to said system bus and local bus in order to transfer data therebetween.

19. A data transferring apparatus for transferring liquid ejection data as claimed in claim 18, wherein an ASIC comprises registers of said main memory, said decode unit and said liquid ejecting head as a circuit block respectively, and registers of said decode unit and said liquid ejecting head are coupled through an dedicated bus in said ASIC.

20. A data transferring apparatus for transferring liquid ejection data as claimed in claim 19, wherein said line buffer comprises two faces of buffer areas capable of storing developed data of predetermined words, liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas while liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when developed data of predetermined words has been accumulated, and developed data is DMA-transferred to said local memory per predetermined words when developed data of predetermined words has been accumulated.

21. A data transferring apparatus for transferring liquid ejection data as claimed in claim 20, wherein data transfers with respect to said local bus from said decode circuit to said local memory and from said local memory to a register of said liquid ejecting head are performed in a burst transfer.

22. A data transferring apparatus for transferring liquid ejection data as claimed in claim 21, wherein said compressed liquid ejection data is run length compressed data, and said decode circuit

can perform hardware development on run length compressed data.

23. A data transferring apparatus for transferring liquid ejection data as claimed in claim 22, wherein said decode unit comprises a non-development processing means for storing uncompressed liquid ejection data DMA-transferred from said main memory in said line buffer without hardware development by said decode circuit.

24. A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data comprising:

- a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;

- a line buffer for storing liquid ejection data developed by said decode circuit per word unit;

- a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit, DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially; and

- a data rearranging means for storing data in an array direction of a bitmap for a liquid ejecting head corresponding to a nozzle array of a liquid ejecting head in said local memory, when data developed in said line buffer is DMA-transferred to a bitmap area of said local memory per word unit.

25. A data transferring apparatus for transferring liquid

ejection data, comprising:

a decode unit comprising a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;

a line buffer for storing liquid ejection data developed by said decode circuit per word unit and a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit; and

DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially,

wherein said decode unit comprises a data dividing means for storing data in bitmap areas which are different per predetermined words, when data developed in said line buffer is DMA-transferred to a bitmap area of said local memory per word unit.

26. A data transferring apparatus for transferring liquid ejection data as claimed in claim 25, wherein said data dividing means sets the number of bitmap areas to be divided in accordance with a ratio of the resolution of liquid ejection data and the resolution of said liquid ejecting head.

27. A data transferring apparatus for transferring liquid ejection data as claimed in claim 26, wherein said data transferring apparatus comprises an invalid data mask processing means for nullifying data from head data, as many bytes as a remainder resulting from dividing a value of a data starting address of

compressed liquid ejection data by the number of data bytes which said system bus can transfer per one data transfer, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

28. A data transferring apparatus for transferring liquid ejection data as claimed in claim 26, wherein said data transferring apparatus comprises an invalid data mask processing means for nullifying head data of one byte in case data starting address of compressed data stored in said main memory is an odd address, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

29. A data transferring apparatus for transferring liquid ejection data as claimed in claim 28, wherein said decode unit comprises a data storage starting position shifting means for storing liquid ejection data developed by said decode circuit from a first byte of said line buffer in a state where a 0-th byte of said line buffer is vacant.

30. A data transferring apparatus for transferring liquid ejection data as claimed in claim 29, wherein said decode unit comprises a data storage ending position shifting means for transferring developed liquid ejection data stored in said line buffer to liquid ejecting head each time developed data of said predetermined words from which one byte has been subtracted is stored in said line buffer.

31. A data transferring apparatus for transferring liquid ejection data as claimed in claim 30, wherein said data transferring apparatus comprises two independent buses which are said system

bus and a local bus, said main memory coupled to said system bus, capable of transferring data and said local memory coupled to said local bus, capable of transferring data, and said decode unit is coupled to said system bus and local bus in order to transfer data therebetween.

32. A data transferring apparatus for transferring liquid ejection data as claimed in claim 31, wherein an ASIC comprises registers of said main memory, said decode unit and said liquid ejecting head as a circuit block respectively, and registers of said decode unit and said liquid ejecting head are coupled through an dedicated bus in said ASIC.

33. A data transferring apparatus for transferring liquid ejection data as claimed in claim 32, wherein said line buffer comprises two faces of buffer areas capable of storing developed data of predetermined words, liquid ejection data developed by the decode circuit is sequentially stored in a first face of the buffer areas while liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when developed data of predetermined words has been accumulated, and developed data is DMA-transferred to said local memory per predetermined words when developed data of predetermined words has been accumulated.

34. A data transferring apparatus for transferring liquid ejection data as claimed in claim 33, wherein data transfers with respect to said local bus from said decode circuit to said local memory and from said local memory to a register of said liquid ejecting head are performed in a burst transfer.

35. A data transferring apparatus for transferring liquid ejection data as claimed in claim 34, wherein said compressed liquid ejection data is run length compressed data, and said decode circuit can perform hardware development on run length compressed data.

36. A data transferring apparatus for transferring liquid ejection data as claimed in claim 35, wherein said decode unit comprises a non-development processing means for storing uncompressed liquid ejection data DMA-transferred from said main memory in said line buffer without hardware development by said decode circuit.

37. A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data comprising:

- a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;

- a line buffer for storing liquid ejection data developed by said decode circuit per word unit;

- a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit, DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially; and

- a data dividing means for storing data in bitmap areas which are different per predetermined words, when data developed in said line buffer is DMA-transferred to a bitmap area of said local memory per word unit.

38. A data transferring apparatus for transferring liquid ejection data, comprising:

a decode unit comprising a decode circuit performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;]

a line buffer for storing liquid ejection data developed by said decode circuit per word unit and a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit; and

DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially,

wherein said decode unit comprises a data storage starting position shifting means for storing liquid ejection data developed by said decode circuit from a first byte of said line buffer in a state where a 0-th byte of said line buffer is vacant.

39. A data transferring apparatus for transferring liquid ejection data, comprising:

a decode unit comprising a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;

a line buffer for storing liquid ejection data developed by said decode circuit per word unit and a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit;

and

DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially,

wherein said decode unit comprises a data storage ending position shifting means for transferring developed liquid ejection data stored in said line buffer to liquid ejecting head each time developed data of said predetermined words from which one byte has been subtracted is stored in said line buffer.

40. A data transferring apparatus for transferring liquid ejection data as claimed in claim 38, wherein said decode unit comprises a data storage ending position shifting means for transferring developed liquid ejection data stored in said line buffer to liquid ejecting head each time developed data of said predetermined words from which one byte has been subtracted is stored in said line buffer.

41. A data transferring apparatus for transferring liquid ejection data as claimed in claim 40, wherein said data transferring apparatus comprises an invalid data mask processing means for nullifying data from head data, as many bytes as a remainder resulting from dividing a value of a data starting address of compressed liquid ejection data by the number of data bytes which said system bus can transfer per one data transfer, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

42. A data transferring apparatus for transferring liquid ejection data as claimed in claim 40, wherein said data transferring

apparatus comprises an invalid data mask processing means for nullifying head data of one byte in case data starting address of compressed data stored in said main memory is an odd address, with respect to word data including head data of compressed data DMA-transferred from said main memory to said decode circuit.

43. A data transferring apparatus for transferring liquid ejection data as claimed in claim 42, wherein said data transferring apparatus comprises two independent buses which are said system bus and a local bus, said main memory coupled to said system bus, capable of transferring data and said local memory coupled to said local bus, capable of transferring data, and said decode unit is coupled to said system bus and local bus in order to transfer data therebetween.

44. A data transferring apparatus for transferring liquid ejection data as claimed in claim 43, wherein an ASIC comprises registers of said main memory, said decode unit and said liquid ejecting head as a circuit block respectively, and registers of said decode unit and said liquid ejecting head are coupled through an dedicated bus in said ASIC.

45. A data transferring apparatus for transferring liquid ejection data as claimed in claim 44, wherein said line buffer comprises two faces of buffer areas capable of storing developed data of predetermined words, liquid ejection data developed by the decode circuit is sequentially stored in a first face of the buffer areas while liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when developed data of predetermined words has been accumulated, and developed data is DMA-transferred to said local

memory per predetermined words when developed data of predetermined words has been accumulated.

46. A data transferring apparatus for transferring liquid ejection data as claimed in claim 45, wherein data transfers with respect to said local bus from said decode circuit to said local memory and from said local memory to a register of said liquid ejecting head are performed in a burst transfer.

47. A data transferring apparatus for transferring liquid ejection data as claimed in claim 46, wherein said compressed liquid ejection data is run length compressed data, and said decode circuit can perform hardware development on run length compressed data.

48. A data transferring apparatus for transferring liquid ejection data as claimed in claim 47, wherein said decode unit comprises a non-development processing means for storing uncompressed liquid ejection data DMA-transferred from said main memory in said line buffer without hardware development by said decode circuit.

49. A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data comprising:

- a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;

- a line buffer for storing liquid ejection data developed by said decode circuit per word unit;

- a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from

said main memory to said decode circuit, DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially; and

a data storage starting position shifting means for storing liquid ejection data developed by said decode circuit from a first byte of said line buffer in a state where a 0-th byte of said line buffer is vacant.

50. A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data comprising:

a decode circuit capable of performing hardware development on liquid ejection data, which is DMA-transferred per word unit from a main memory via a system bus, compressed to be capable of line development;

a line buffer for storing liquid ejection data developed by said decode circuit per word unit;

a DMA-transferring means for DMA-transferring liquid ejection data compressed to be capable of line development from said main memory to said decode circuit, DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejecting head sequentially; and

a data storage ending position shifting means for transferring developed liquid ejection data stored in said line buffer to liquid ejecting head each time developed data of said predetermined words from which one byte has been subtracted is stored in said line buffer.